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Application No. 10/711,653  
Technology Center 2824  
Amendment dated July 5, 2007  
Reply to Office Action dated February 12, 2007

**REMARKS**

As of the filing of the present Office Action, claims 1-43 were pending in the above-identified US Patent Application. In the Office Action, the Examiner withdrew claims 18-27 from consideration due to a restriction requirement, rejected claims 2, 3, 6, and 10 under 35 USC §112, second paragraph, rejected claims 1-17, 28-36, and 41-43 under 35 USC §102, and deemed claims 37-40 (which depend from claim 28) to recite allowable subject matter.

In the present response, Applicants have amended the claims as set forth above. More particularly:

Independent claim 1 and its remaining dependent claims have been amended for consistency with each other, including use the phrase "input voltage supplying means" instead of "supply means," the former of which clearly finds antecedence based on the phrase "means for supplying an input voltage" in claim 1.

Independent claims 1 and 28 have been amended to specify that the apparatus/method increases power to a memory module installed in a first of a plurality of memory slots, and that the input voltage supplying means (10) is linked to a memory bus of the memory subsystem to deliver an input voltage

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to the memory module. Support for these amendments can be found in Applicants' specification at [Para 25].

Independent claim 1 has also been amended to specify that the input voltage supplying means (10) comprises a portion (e.g., pins 24) configured to plug directly into an available memory slot of the memory subsystem. Support for this amendment can be found in original claims 2 and 3 (the latter of which has been canceled without prejudice) and Applicants' specification at [Para 30].

In view of the amendment to its parent claim 1, dependent claim 2 has been amended to recite a limitation that finds support in Applicants' specification at [Para 14].

Claims 18-27 have been canceled without prejudice to Applicants in view of the above-noted restriction requirement, for the purpose of reducing and simplifying the issues remaining in the examination of Applicants' application.

Applicants believe that the above amendments do not present new matter. Favorable reconsideration and allowance of remaining claims 1, 2, 4-17 and 28-43 are respectfully requested in view of the above amendments and the following remarks.

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**Rejections under 35 USC §112, Second Paragraph**

Under this rejection, claims 2, 3, 6, 10, and 12-16 were rejected as indefinite. Rejections of claims 6, 10, and 12-16 concerning "supply means" are believed overcome by the above-noted amendments to claims 1, 6, 10, and 12-16. Rejections of claims 2 and 3 are rendered moot by their respective amendment and cancellation.

In view of the above, withdrawal of the rejections under 35 USC §112, second paragraph, is respectfully requested.

**Rejection under 35 USC §102**

Remaining claims 1, 2, 4-17, 28-36, and 41-43 were rejected as being anticipated by U.S. Patent 7,143,298 to Wells et al. (Wells). In setting forth the rejection, the Examiner explained that Wells discloses

an apparatus as shown in figures 1-7 comprising: a memory subsystem (memory card (10, column 2, line 30) connected to a motherboard (column 3, lines 10-12); means for (a battery 18, a pump 28, and VRM 22) supplying an input voltage to the memory subsystem (10) at a level (5V) that is higher than a power level provided to the memory subsystem by the motherboard (3.3V), the memory subsystem (10) having pins/terminals (30) connected to a slot in the motherboard to excess of [sic] available voltage to the motherboard.

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Applicants respectfully disagree, because the apparatus taught by Wells differs from Applicants' claimed invention in a number of significant aspects.

A "memory subsystem" is not a memory module (card), but a combination of memory modules associated with a motherboard of a computer. Amended independent claims 1 and 28 specify that an "input voltage supplying means" (10) or "supply means" (10), respectively, is able to be inserted into a vacant memory slot, and consequently uses the shared power and ground plane of all memory slots, with the result that an input voltage generated by the supplying/supply means (10) is supplied to individual memory modules sharing the same power and ground topology by reverse powering the memory subsystem under normal operating conditions of the computer. This supplying/supply means (10) can receive power from an external power source, such as the ATX system power supply or a power source external to the entire computer. The power received by the supply means (10) is then transformed, for example, to a user-selected value, that can be and is typically above that of the memory supply voltage supplied by the motherboard. The increased supply voltage can then be the basis for increasing the operating frequency of the memory modules inserted into the remaining slots of the motherboard beyond the frequency that can be obtained

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under normal voltage supply situations. The boosted power supply inserted in the vacant memory slot does not need or even desirably contain any memory chips that functionally contribute to the system memory.

In contrast, Wells describes a memory module 10 with memory chips 12, in addition to a back-up powering capability that makes use of a battery 18, capacitor 20, voltage regulator 22, and charge pump 28. While the capacitor 20 may be "charged up to 5 volts rather than 3.3 volts" (column 4, lines 57-59) with the charge pump 28 (column 4, lines 59-64), the power supplied to the memory chips 12 is not at 5 volts. Instead, Wells clearly states that the "[m]odule requires a regulated 3.3 volt supply voltage" (column 4, lines 32-33; emphasis added) and the "the motherboard main 3.3 volt power supply is combined with battery 18 as an input to voltage regulator 22 to supply a 3.3 volt output voltage to supply SDRAM 12" (column 4, lines 35-38; emphasis added). Because Wells discloses the module 10 as requiring a 3.3 supply voltage and the motherboard as supplying a 3.3 volt power supply, Wells cannot be relied on for disclosing or even suggesting Applicants' apparatus, in which "an input voltage [is supplied] to the memory module of the memory subsystem at a level that is higher than a power level provided to the memory subsystem by the motherboard."

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In view of the above, the purpose, mode of operation, and physical implementation described by Wells does not disclose or suggest Applicants' claimed subject matter.

Specifically regarding the method of independent claim 28, the Examiner cited Wells as disclosing

electrically connecting a supply means (3.3V) to an available memory slot of the memory subsystem;  
                  electrically connecting a power source (by a cable) to the supply means; and  
                  delivering an input voltage (18,22,28) to a memory subsystem (10) with the supply means.

As now amended, claim 28 requires "providing power to at least one memory module in at least a first of a plurality of memory slots of a memory subsystem of a computer," including "electrically connecting a supply means to an available memory slot of the memory subsystem; . . ." The distinction here is that Wells' back-up powering capability is for the memory module 10 (and its memory chips 12) on which the battery 18, capacitor 20, voltage regulator 22, and charge pump 28 are mounted - and is not installed in an available (and therefore different) memory slot than the module 10.

As to claim 6, a text search of Wells did not find any use of the word "cable" in any instance, particularly in reference to a cable that directly

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connects a memory module to an external power source.

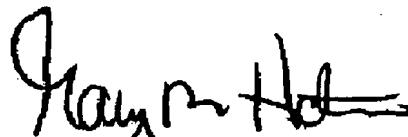
In view of the above, withdrawal of the rejection under 35 USC §102  
is respectfully requested.

**Closing**

For all of the above reasons, Applicants believes that the rejections of their claims have been overcome, and that the claims define patentable novelty over all the references, alone or in combination, of record. It is therefore respectfully requested that this patent application be given favorable reconsideration.

Should the Examiner have any questions with respect to any matter now of record, Applicants' representative may be reached at (219) 462-4999.

Respectfully submitted,



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Attachment: Petition for Extension of Time